Customer No.: 31561
Application No.: 10/064,799
Docket No.: 9222-US-PA

REMARKS

Present Status of the Application

The Office Action rejected claims 1-5 under 35 U.S.C. 102(b), as being anticipated by Sogawa et al.(US Patent No. 5,670,402). Claims 6-17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US Patent No. 6,146,949) in view of Sogawa et al.. Claims 1, 6, 11 and 17 have been amended for clarification purposes. This Amendment is promptly filed to place the above-captioned case in condition for allowance. No new matter has been added to the application by the amendments made to the claims, specification or otherwise in the application. After considering the following remarks, a notice of allowance is respectfully solicited.

Discussion of 102 and 103 Rejections

Claims 1-5 stand rejected under 35 U.S.C. 102(b), as being anticipated by Sogawa et al.(US Patent No. 5,670,402).

Claims 6-17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US Patent No. 6,146,949) in view of Sogawa et al..

Applicants respectfully traverse the rejections for at least the reasons set forth below.

The independent claims 1 and 6 have been amended to more clearly define the device and the fabrication method according to the present invention. No new matter has been added to the application by the amendments made to the claims, and the supporting grounds for the amendment can be found at least in Figs. 2E-2G. After removing the cap layer 206a, the

conductive structure 204a is exposed, as shown in Fig. 2F. From Fig. 2G, it clearly shows that the word line 220 is disposed on the gate 204b and the insulation layer 218 after patterning the conductive layer and the conductive structure 204a.

As amended, claims 1 and 6 respectively recite:

1. A memory device, comprising
a substrate;
a gate oxide layer, disposed on a surface of the substrate;
a gate, disposed on a portion of the gate oxide layer;
a buried drain line, located in the substrate beside both sides of the gate;
a spacer, disposed on sidewalls of the gate;
a deep doped region, located in the substrate below a part of the buried drain line, wherein the buried drain line and the deep doped region together form a bit line of the memory device;
an insulation layer, disposed on the gate oxide layer and above the bit line; and
a word line, disposed on the gate and the insulation layer, perpendicular to a direction of the bit line.

6. A fabrication method for a memory device, comprising:
forming a gate oxide layer on a substrate;
forming a bar-shaped conductive structure on the gate oxide layer, wherein a cap layer is formed on a top of the bar-shaped conductive structure;
forming a buried drain line in the substrate beside both sides of the bar-shaped conductive structure;
forming a spacer on sidewalls of the bar-shaped conductive structure and the cap layer after forming the buried drain line;
forming a deep doped region in the substrate beside both sides of the spacer, wherein the buried drain line and the deep doped region together form a bit line of the memory device;
forming an insulation layer on the gate oxide layer and above the bit line;
removing the cap layer;
forming a conductive layer on the bar-shaped conductive structure and the insulation layer and over the substrate; and
patterning the conductive layer and the bar-shaped conductive structure in a direction perpendicular to a direction of the bit line to form a word line and a plurality of gates.

(Emphasis added)

Applicant respectfully asserts that the memory device claimed in the present invention patentably distinguishes over Sogawa's structure, because Sogawa lacks the features emphasized above in claim 1 (in bold). Especially, Sogawa fails to disclose the gate as claimed in claim 1.

Sogawa discloses a semiconductor structure including diffusion regions 22a/22d arranged alternately in parallel with each other, insulation film 24 on each of the diffusion regions 22s/22d, gate oxide film 26 on the substrate 20, and word line layer 28 on the insulation film 24 and the gate oxide film 26. Obviously, Sogawa does not teach or suggest the gate structure as claimed in claim 1 and the present invention. As explained in Sogawa's Figs. 4a-4g, the oxide spacer 38 is formed on a side wall of each of the silicon oxide film 30 and the silicon nitride film 32 by etching back (Col. 6, lines 8-13). Further, after removing the silicon oxide film 30 and the silicon nitride film 32, a gate oxide film 26 is formed on the exposed surface of the substrate 20 and later the polysilicon word line layer 28 is deposited **on the gate oxide film 26,** as shown in Fig. 4g. Even if considering Sogawa's word line layer 28 is comparable to the word line of the present invention, it is self-evident that Sogawa in no way teaches or suggest the gate on a portion of the gate oxide layer in the present invention. Accordingly, Sogawa fails to disclose the spacer on sidewalls of the gate and the word line on the gate.

Therefore, Sogawa fails to teach or suggest each and every feature as claimed in the present invention. As a result, Sogawa did not anticipate the present invention as suggested by the Office Action, to arrive at the present invention as recited in independent claim 1.

As noted by the Office Action, Wu fails to disclose forming a deep doped region in the substrate beside both sides of the spacer, wherein the buried drain line and the deep doped region together form a bit line of the memory device.

Wu discloses performing implantation to form buried bit lines 14 after forming silicon oxide spacers 12. Clearly, Wu does not teach or suggest "forming a spacer on sidewalls of the bar-shaped conductive structure and the cap layer after forming the buried drain line", as claimed in claim 6.

In addition, Wu teaches forming a borophosphosilicate glass (BPSG) layer 16 and performing a high temperature anneal to reflow the BPSG layer 16, after the formation of buried bit line 14. Wu further emphasizes "the thermal anneal is used to active the dopant, thereby forming buried bit lines profile" (col. 4, lines 45-46). Therefore, Wu teaches performing a thermal anneal after forming the buried bit lines 14.

Similarly, Sogawa discloses forming gate oxide film 26 by thermal oxidation after implanting ions 40 into the substrate. Sogawa stresses that the ion implanted in the substrate is activated in a process of heat treatment for forming the gate oxide film 26 so that diffusion regions 22d and 22s are formed (col. 6, lines 45-52).

On the contrary, in the present invention, the buried drain line is formed after the formation of the gate oxide layer and the conductive structure, so that the diffusion effect in the buried drain line due to the high temperature when forming the gate oxide layer and the

conductive structure is mitigated. According to the method of this invention, the buried drain line can be shallow to prevent the short channel effect and the junction leakage problems.

Obviously, neither Wu nor Sogawa recognizes the advantages of this invention and try to solve the problems this invention tried to solve.

The Office Action asserts it obvious to modify the method disclosed by Wu to include Sogawa's step of forming a deep doped region, in order to increase reading speed of data, as disclosed by Sogawa.

However, as stated by Sogawa, the thick insulation layer is deposited between the bit line layer and the word line layer, so that the capacitance there-between is reduced and the reading speed is increased. Sogawa teaches forming thick insulation layer to help increasing the reading speed.

Since none of these two references recognize the advantages of this invention and both references fail to teach or suggest the combination of features recited in independent claims, there is no motivation to combine Wu with Sogawa as suggested by the Office Action. Therefore, Applicant respectfully submits that independent claim 6 patentably distinguishes over Wu and Sogawa, either alone or in combination. Depend claims are allowable for at least the reasons stated with regard to their respective base claims.

As a result, reconsideration and withdrawal of these 102 and 103 rejections are respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: bclinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw